What is claimed is:

1. A new grid metal design for image sensors comprising:

a semiconductor image sensor chip having a pixel region covering most of the chip and a logic circuit region on the chip periphery, the pixel region containing an array of image pixels where for each image pixel the majority of its area is occupied by a light sensing element and the other image pixel circuit elements are arranged in the periphery of the image pixel without overlapping the image sensing element;

a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

a number of metal levels of the second type, where in each of said levels of the second type functional patterns exist only for the chip peripheral logic circuits and dummy metal patterns cover the pixel region except for the light sensing elements;

a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

2. The design of Claim 1 wherein the array of image pixels is a grid matrix array.

3. The design of Claim 1 wherein the number of metal levels of the first type is between one and four.

4. The design of Claim 1 wherein the number of metal levels of the second type is between one and four.

5. The design of Claim 1 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

6. The design of Claim 1 wherein the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

7. A method of fabricating a new grid metal design for image sensors comprising:

providing a partially processed semiconductor wafer having chips in which are partially formed image sensors, said partially formed image sensor chips having pixel regions and chip peripheral logic circuit regions, the pixel region containing an array of image pixels and where for each image pixel of a pixel region the majority of its area is occupied by a light sensing element and the other image pixel elements are arranged in the periphery of the image pixel so as not to cover the light sensing element.

forming a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

forming a number of metal levels of the second type, where in each of said levels of the second type functional patterns exist only for the chip peripheral logic circuits and dummy metal patterns cover the pixel region except for the light sensing elements;

forming a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

8. The method of Claim 7 wherein the array of image pixels is a grid matrix array.

9. The method of Claim 7 wherein the number of metal levels of the first type is between one and four.

10. The method of Claim 7 wherein the number of metal levels of the second type is between one and four.

11. The method of Claim 7 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

12. The method of Claim 7 wherein the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

13. A new grid metal design for CMOS image sensors comprising:

a semiconductor image sensor chip having a pixel region covering most of the chip and a logic circuit region on the chip periphery, the pixel region containing an array of image pixels where for each image pixel the majority of its area is occupied by a light sensing element and the other image pixel circuit elements are arranged in the periphery of the image pixel without overlapping the image sensing element;

a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

a number of metal levels of the second type, where in each of said levels of the second type functional patterns exist only for the chip peripheral logic circuits and dummy metal patterns cover the pixel region except for the light sensing elements;

a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

14. The design of Claim 13 wherein the light sensing element is a photodiode.

15. The design of Claim 13 wherein the array of image pixels is a grid matrix array.

16. The design of Claim 13 wherein the number of metal levels of the first type is between one and four.

17. The design of claim 13 wherein the number of metal levels of the second type is between one and four.

18. The design of Claim 13 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

19. The design of Claim 13 wherein the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

20. A method of fabricating a new grid metal design for CMOS image sensors comprising:

providing a partially processed semiconductor wafer having chips in which are partially formed image sensors, said partially formed image sensor chips having pixel regions and chip peripheral logic circuit regions, the pixel region containing an array of image pixels and where for each image pixel of a pixel region the majority of its area is occupied by a light sensing element and the other image pixel elements are arranged in the periphery of the image pixel so as not to cover the light sensing element.

forming a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

forming a number of metal levels of the second type, where in each of said levels of the second type functional patterns exist only for the chip peripheral logic circuits and dummy metal patterns cover the pixel region except for the light sensing elements;

forming a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

21. The method of Claim 20 wherein the light sensing element is a photodiode.

22. The method of Claim 20 wherein the array of image pixels is a grid matrix array.

23. The method of Claim 20 wherein the number of metal levels of the first type is between one and four.

24. The method of Claim 20 wherein the number of metal levels of the second type is between one and four.

25. The method of Claim 20 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

26. The method of Claim 20 wherein the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

27. A new grid metal design for bipolar image sensors comprising:

a semiconductor image sensor chip having a pixel region covering most of the chip and a logic circuit region on the chip periphery, the pixel region containing an

array of image pixels where for each image pixel the majority of its area is occupied by a light sensing element and the other image pixel circuit elements are arranged in the periphery of the image pixel without overlapping the image sensing element;

a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

a number of metal levels of the second type, where in each of said levels of the second type functional patterns exist only for the chip peripheral logic circuits and dummy metal patterns cover the pixel region except for the light sensing elements;

a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

28. The design of Claim 27 wherein the light sensing element is an emitter-base junction of a bipolar transistor.

29. The design of Claim 27 wherein the array of image pixels is a grid matrix array.

30. The design of Claim 27 wherein the number of metal levels of the first type is between one and four.

31. The design of claim 27 wherein the number of metal levels of the second type is between one and four.

32. The design of Claim 27 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

33. The design of Claim 27 wherein the dielectric and passivation levels are composed of

dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.

34. A method of fabricating a new grid metal design for bipolar image sensors comprising:

providing a partially processed semiconductor wafer having chips in which are partially formed image sensors, said partially formed image sensor chips having pixel regions and chip peripheral logic circuit regions, the pixel region containing an array of image pixels and where for each image pixel of a pixel region the majority of its area is occupied by a light sensing element and the other image pixel elements are arranged in the periphery of the image pixel so as not to cover the light sensing element.

forming a number of metal levels of the first type, where at each of the levels of the first type functional patterns exist both for the chip peripheral logic circuits and for the pixel circuit elements;

forming a number of metal levels of the second type, where in each of said levels of the second type functional patterns exist only for the chip peripheral logic circuits and dummy metal patterns cover the pixel region except for the light sensing elements;

forming a first dielectric layer under the first metal layer, an interlevel dielectric layer between said metal levels of either type and a passivation layer over the last metal level.

35. The method of Claim 34 wherein the light sensing element is an emitter-base junction of a bipolar transistor.

36. The method of Claim 34 wherein the array of image pixels is a grid matrix array.

37. The method of Claim 34 wherein the number of metal levels of the first type is between one and four.

38. The method of Claim 34 wherein the number of metal levels of the second type is between one and four.

39. The method of Claim 34 wherein the metal levels of the first type and of the second type are composed of either copper, gold, aluminum, cobalt or tungsten or of composites of these metals or of metal silicides.

40. The method of Claim 34 wherein the dielectric and passivation levels are composed of dielectric materials such as silicon oxide, silicon nitride or silicon oxynitride.